CLAIMS

1. A light-emitting thyristor matrix array wherein an array of three-terminal light-emitting thyristors in which a substrate is used as a common cathode or anode is divided into blocks n by n (n is an integer $\geqq 2$), gates of n light-emitting thyristors included in each block are separately connected to n gate-selecting lines, and anodes or cathodes of n light-emitting thyristors included in each block are commonly connected to one terminal, respectively, characterized in that :

a wiring layout where wirings not to be electrically shorted are crossed is implemented by a two-layer wiring structure.

2. A light-emitting thyristor matrix array wherein an array of three-terminal light-emitting thyristors in which a substrate is used as a common cathode or anode is divided into blocks n by n (n is an integer $\geqq 2$), anodes or cathodes of n light-emitting thyristors included in each block are separately connected to n anode-selecting lines or cathode-selecting lines , and gates of n light-emitting thyristors included in each block are commonly connected to one terminal, respectively, characterized in that :

a wiring layout where wirings not to be electrically shorted are crossed is implemented by a two-layer wiring structure.

3. A light-emitting thyristor matrix array wherein an array of three-terminal light-emitting thyristors in which a substrate is used as a common cathode or anode is divided

into blocks n by n (n is an integer $\geqq 2$), gates of n light-emitting thyristors included in each block are separately connected to n gate-selecting lines, and anodes or cathodes of n light-emitting thyristors included in each block are commonly connected to one terminal, respectively, characterized in that :

a wiring layout where wirings not to be electrically shorted are crossed is implemented by utilizing gate electrodes of the light-emitting thyristors as cross under wirings.

4. A light-emitting thyristor matrix array wherein an array of three-terminal light-emitting thyristors in which a substrate is used as a common cathode or anode is divided into blocks n by n (n is an integer $\geqq 2$), anodes or cathodes of n light-emitting thyristors included in each block are separately connected to n anode-selecting lines or cathode-selecting lines , and gates of n light-emitting thyristors included in each block are commonly connected to one terminal, respectively, characterized in that :

a wiring layout where wirings not to be electrically shorted are crossed is implemented by utilizing anode electrodes or cathode electrodes of the light-emitting thyristors as cross under wirings.

5. A light-emitting thyristor matrix array wherein an array of three-terminal light-emitting thyristors in which a substrate is used as a common cathode or anode is divided into blocks n by n (n is an integer $\geqq 2$), gates of n light-emitting thyristors included in each block are separately

connected to n gate-selecting lines, and anodes or cathodes of n light-emitting thyristors included in each block are commonly connected to one terminal, respectively, characterized in that :

bonding pads are arrayed in parallel with the array direction of the light-emitting thyristors and on one side of the array of the light-emitting thyristors, and

a wiring layout where wirings to the bonding pads cross the gate-selecting lines is implemented by utilizing electrodes on islands isolated from the light-emitting thyristors as cross under wirings.

6. The light-emitting thyristor matrix array of claim 5, wherein the electrodes on the islands isolated from the light-emitting thyristors are gate electrodes, anode electrodes, or cathode electrodes.

7. The light-emitting thyristor matrix array of claim 5, wherein the anode electrode or cathode electrode is utilized as the cross under wiring, the anode electrode or cathode electrode is electrically shorted to the gate electrode on the same isolated island.

8. A light-emitting thyristor matrix array wherein an array of three-terminal light-emitting thyristors in which a substrate is used as a common cathode or anode is divided into blocks n by n (n is an integer $\geqq 2$), gates of n light-emitting thyristors included in each block are separately connected to n gate-selecting lines, and anodes or cathodes of n light-emitting thyristors included in each block are

commonly connected to one terminal, respectively, characterized in that :

SUB A1

bonding pads are arrayed in parallel with the array direction of the light-emitting thyristors and on one side of the array of the light-emitting thyristors, and

a wiring layout where wirings to the bonding pads cross the gate-selecting lines is implemented by utilizing gate electrode elongated around a light-emitting portion of the thyristor as a cross under wiring.

9. A light-emitting thyristor matrix array wherein an array of three-terminal light-emitting thyristors in which a substrate is used as a common cathode or anode is divided into blocks n by n (n is an integer $\geqq 2$), gates of n light-emitting thyristors included in each block are separately connected to n gate-selecting lines, and anodes or cathodes of n light-emitting thyristors included in each block are commonly connected to one terminal, respectively, characterized in that :

bonding pads are arrayed in parallel with the array direction of the light-emitting thyristors and on one side of the array of the light-emitting thyristors, and

a wiring layout where wirings to the bonding pads cross the gate-selecting lines is implemented by utilizing two gate electrode parts provided around a light-emitting portion of the thyristor as a cross under wiring, the two gate electrode parts being electrically connected by an underlying gate layer.

10. A light-emitting thyristor matrix array wherein an array

of three-terminal light-emitting thyristors in which a substrate is used as a common cathode or anode is divided into blocks n by n (n is an integer $\geqq 2$), anodes or cathodes of n light-emitting thyristors included in each block are separately connected to n anode-selecting lines or cathode-selecting lines , and gates of n light-emitting thyristors included in each block are commonly connected to one terminal, respectively, characterized in that :

bonding pads are arrayed in parallel with the array direction of the light-emitting thyristors and on one side of the array of the light-emitting thyristors, and

a wiring layout where wirings to the bonding pads cross the anode-selecting lines or cathode-selecting lines is implemented by utilizing electrodes on islands isolated from the light-emitting thyristors as cross under wirings.

11. The light-emitting thyristor matrix array of claim 10, wherein the electrodes on the islands isolated from the light-emitting thyristors are gate electrodes, anode electrodes, or cathode electrodes.

12. The light-emitting thyristor matrix array of claim 11, wherein the anode electrode or cathode electrode is utilized as the cross under wiring, the anode electrode or cathode electrode is electrically shorted to the gate electrode on the same isolated island.